IDEC Chip Design Contest

A 2.4 GHz Fractional-N Sub-Sampling PLL with Phase-Interpolator linked DTC

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Introduction

The conventional PLL has been widely used in the transceivers. But it has drawbacks of the in-band phase noise. Owing to the existence of divide-by-N in a feedback path, PFD/CP and the divider noise in power are divided by N^2 when transferred to the output of conventional PLL. Therefore, conventional PLL's in-band phase noise is confined by divide-by-N. For this reason, it is hard to design PLL with a low jitter. A sub-sampling PLL architecture can work without a divider unlike the conventional PLL. Thus, divider noise and the power dissipation can be eliminated. In addition to the removal of the divider noise, compared with conventional PLL, PD/CP of the sub-sampling PLL noise is not multiplied by N^2. Then, the in-band phase noise is significantly alleviated, so that we can design PLL with very low jitter as well as low power. With many details, the analysis of fractional mode SSPLL is implemented with the proposed hybrid type phase-interpolator. And a sign-sign Least Mean Square (LMS) algorithm is used to calibrate the linearity of the SSPLL with Spectre.

Hybrid-Phase Interpolator

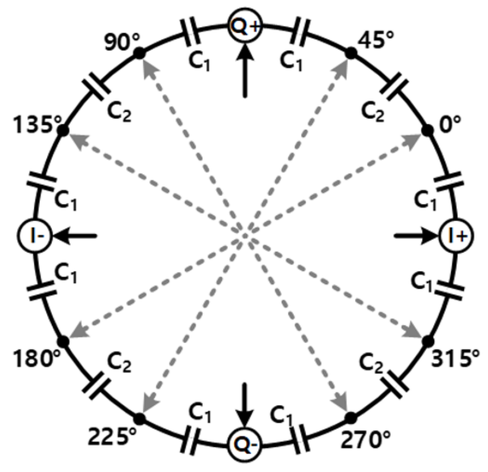

Fig. 1. Schematic of the capacitive PI.

For the implementation of a fractional mode PLL with the sub-sampling technique, the multi-phase clock signal is needed. Fig. 1 represents the circuit schematic of the capacitive PI. It makes the half-quadrature output signals from quadrature excitations. This technique creates a multi-phase by the ratio of C_1 and C_2. If we assume the excellent matching of the on-chip components, we can generate the accurate half quadrature output phases by capacitive PI regardless of process and temperature variations. For the wanted phases, generated multiple output phases from capacitive PI can be selected by a multiplexer.

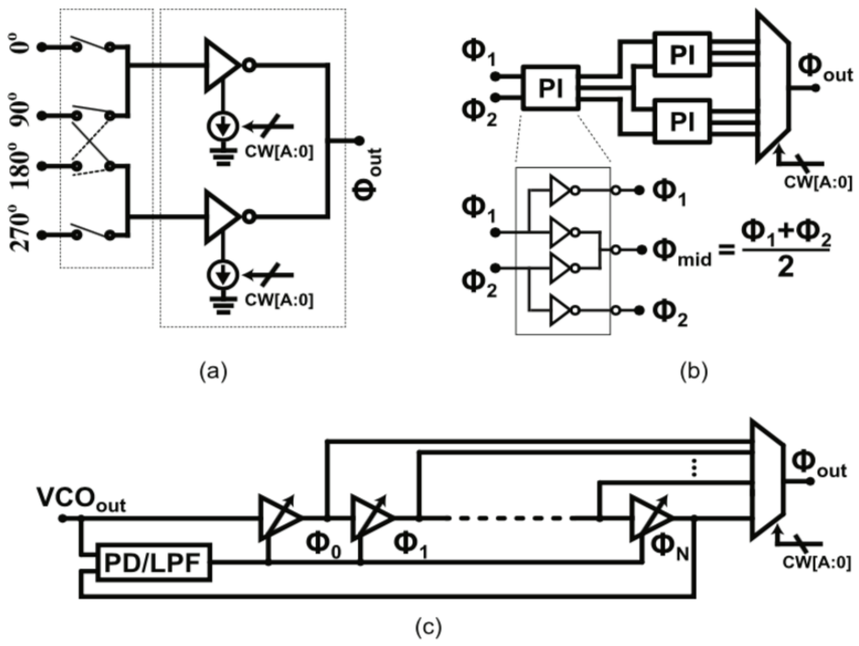

Fig. 2. Various phase-interpolator topologies. (a) current-mode. (b) tournament-type, (c) DLL-based

The active phase-interpolator (PI) has been used to address many different multi-phase generation circuits, as shown in Fig. 2. The current-mode PI and tournament-mode PI shown in Fig, 2(a) and (b) operate on two existing phases to produce an intermediate phase. Fig. 2(c) is a special case of PI and is closer to the DTC family owing to the dependence on a delayed locked loop (DLL) for making multi-phase generation. At the perspective of the linearity, tournament-type PI is better than the current-mode PI and DLL-based PI. Therefore, it is used for generating a multi-phase from the capacitive PI. As a result, using a PI including both the capacitive PI and the tournament-type PI can effectively reduce the dynamic range of the DTC.

This proposed structure relaxes the robust requirements imposed on the DTC in conventional fractional-N PLL by implementing the hybrid phase-interpolator (PI). This PI includes the active and the capacitive PI, which decreases the power consumption compared with the pipelined PI by reducing the unit PI amounts. In addition, it exhibits a lower sensitivity to the parasitic components and mismatches than capacitive PI. It can make efficient structure of the multi-phase generators needed for the fractional-N operation. It also exhibits both low power consumption and low intrinsic jitter.

Conclusion

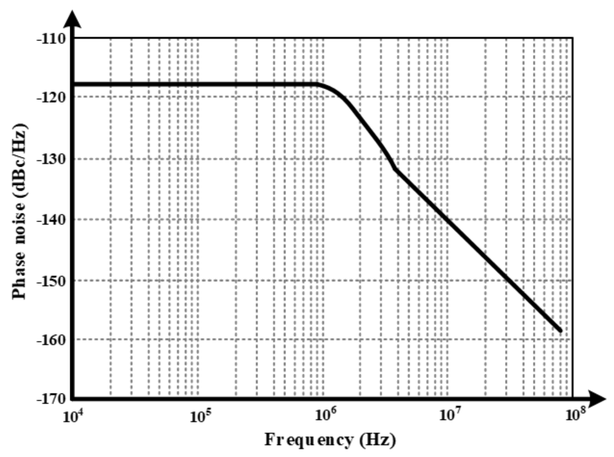

Fig. 3. Simulated PLL output phase noise with Cppsim.

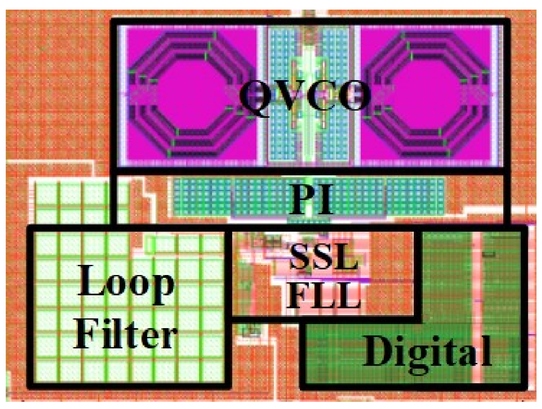

Fig. 4. Top layout.

	This work
Technology (nm)	65
Ref. (MHz)	40
Output Freq. (GHz)	2.2~2.6
In-band PN (dBc/Hz)	-120
Integrated rms Jitter (fs)	162 (10kH-20MHz)
Ref. Spur (dBc)	-73
Frac. Spur (dBc)	-47 (10MHz)
Power (mW)	7
No. of Out. Phase	32
FoM (dB)	-247.3

Fig. 5. Post extraction simulation result of proposed SSPLL

This proposed fractional-N SSPLL is implemented in a 180 nm CMOS process. A 1.0V supply powers this chip. It can tune from 2.2 GHz to 2.6 GHz. Fig.3 shows the simulation result of Cppsim with the result of Spectre. The phase noise at 1 MHz offset of this SSPLL is -118 dBc/Hz in the fractional mode. The loop bandwidth is set to around 1.4 MHz. The simulated rms jitter in fractional mode is 162 fs in the integration range of 10 kHz to 20 MHz. FoM is calculated as -247.3 dB. Fig. 5 shows the post extraction simulation of the proposed SSPLL.

Acknowledgements

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